## REMARKS/ARGUMENTS

Applicants received the final Office Action dated April 15, 2004 in which the Examiner rejected claim 21 as anticipated by Nattkemper (U.S. Pat. No. 5,999,518) and rejected claims 1-20 and 22-24 as obvious over the combination of Nattkemper and Shah (U.S. Pat. No. 6,347,337). Applicants amend claims 14-16 and 21-23. Based on the arguments and amendments contained herein, Applicants believe all pending claims to be in condition for allowance.

Nattkemper is an Alcatel-owned patent directed to telecommunications equipment used, naturally, in the telecommunications industry. Figure 1 discloses a "telecommunications network" 10 that includes a plurality of "switching units" 104. Each switching unit 104 connects to one other switching network 104 via a bidirectional optical connection 108. Col. 3, line 29 through col. 4, line 3. The bidirectional connections 108 permit information to be transmitted "downstream" or "upstream." "The transmission of information may be in the downstream direction, such as from the first switching unit 104a to the intermediate switching unit 104i that it is directly connected to. Similarly, information may be transmitted in the upstream direction, such as from the last switching unit 104a to the intermediate switching unit 104l that it is directly connected to." Col. 4, lines 13-19.

The telecommunications network 10 of Nattkemper is used to facilitate asynchronous transfer mode ("ATM") networks. Col. 2, lines 15-17. "ATM cells" are transmitted between the switching units 104. An ATM cell contains a header and a data payload. See attached print out of web page defining "ATM cell."

> ATM cells include information such as virtual path ("VP") and virtual circuit ("VC") routing information, and information concerning their termination ("terminating information"). Each switching unit 104 analyzes and evaluates the information included with each ATM cell. If the ATM cell identifies VP or VC routing information that is associated with a particular switching unit 104 analyzing the cell, then the cell is forwarded by that particular switching unit to the appropriate destination. Similarly, if the ATM 104 cell includes terminating information that is associated with the particular

> switching unit 104 evaluating the cell, then the cell is terminated by that particular switching unit 104. Col. 4, lines 35-46.

Nattkemper also discloses a "credit-based scheme...to control upstream congestion between the switching units 104." Col. 4, lines 62-65.

> The first switching unit 104a preferably generates a command cell in the downstream direction. The command cell includes information that defines the credits to be awarded to each unit switching 104.... In response to reception of the command cell, the last switching unit 104n generates a feedback status cell, which includes feedback status information, such as the congestion status and behavioral attributes of a given shelf. The feedback status cell is, however, passed upstream and the feedback information therein is modified by the intermediate switching units 104i. Specifically, each intermediate switching unit 104i preferably supplements the information already included in the feedback status cell, which concerns other units, with feedback information concerning that particular unit. Using the information provided for in the command cell, together with the feedback status cell, allows for a credit-based scheme to take place whereby each switching unit 104 is informed of the number of credits it is awarded. The number of credits relates to the number of ATM cells that a switching unit 104 can pass upstream in a given period of time. Upon receiving the credits, a particular switching unit 104 may start to launch ATM cells into the upstream connection 108 until its credits are exhausted.... The master switching unit 104, preferably the first switching unit 104a, should be operable to compute the credits awarded to each slave unit switching 104 based on the command and feedback status cells, and to inform each slave switching unit of its allotted number of credits. As a consequence of the fairness analysis and credit based scheme, the connections 108 between the switching units 104 are regulated such that upstream congestion (i.e., a bottleneck) is avoided. Col. 4, line 65 through col. 5, line 32.

As described above, Nattkemper discloses switching units that pass "ATM cells" back and forth. Each ATM cell contains routing information and a data payload.

Shah is directed to a credit-based flow control scheme over a virtual interface architecture ("VIA") for a system area network. See e.g. Title. Shah relates to communications between computer systems coupled together by way

of a network. The Summary of Shah states:

> [A] method of sending data from a local endpoint system to a remote endpoint system across a network is provided. The local endpoint system includes a plurality of work queues for posting data transfer requests. It is determined if a sufficient number of send credits is available at the local endpoint system. A data packet is sent from the local endpoint system over the network if a sufficient number of send credits are available. Otherwise, if a sufficient number of send credits is not available at the local endpoint system, a credit request packet is sent from the local endpoint system to the remote endpoint system, and the local endpoint system waits for a credit response packet from the remote endpoint system before sending a data packet. Col. 1, line 65 through col. 2, line 11.

Thus, in Shah a source must actively request credits to receive credits to use to send data packets. Accordingly, credits are not automatically provided returned to the source without the source requesting them. A Credit Request message is used to request credits.

Claim 1 is directed to a "multi-processor computer system" that includes a "memory controller configured to accept memory requests from the plurality of processors." The Examiner alleges that Nattkemper discloses the claimed "memory controller" by way of one or more of the controllers shown in Figure 4. Applicants are not clear which controller in Figure 4 the Examiner contends is akin to the claimed memory controller. Clarification is requested. At any rate, none of the controllers 86 shown in Figure 4 are described as being capable of accepting memory requests. With reference to Figure 4, Nattkemper discloses that "cells" are stored in the various queues and managed by the various controllers. See e.g. col. 7, lines 9-33. As explained above, the cells in Nattkemper refer to messages that have a header comprising routing information and a data payload and are used in a telecommunications network. The cells are not described as being memory requests.

Accordingly, Nattkemper does not teach or even suggest a memory controller as is recited in claim 1. Nattkemper does not disclose a memory controller that accepts memory requests. Consequently, Nattkemper does not

disclose a memory controller that accepts memory requests "in a shared buffer using a credit-based allocation scheme." Shah is similarly deficient. At least for these reasons, claim 1 and dependent claims 2-6 are allowable over the art of record.

Claim 7 is directed to a "computer processor" that, among other features, comprises a "memory controller" having a "request buffer" in a directory in-flight table. Further, the claimed processor assigns credits to a "cache control unit" and an "interprocessor and I/O router." The directory in-flight table "immediately returns credits to the source from which the credit was received" as long as "the request buffer is filled below a buffer threshold." The Examiner rejected claim 7 as obvious for "similar reasons" as for claims 1 and 2. Office Action page 7. Neither Nattkemper nor Shah discloses a memory controller that comprises a "directory in-flight table [that] immediately returns credits to the source from which the credit was received." Shah, for example, only returns credits if the source actively request credits.

Nattkemper does not disclose immediately returning credits. Instead, Nattkemper discloses an algorithm by which credits are computed and granted to various switches 104 in such a way so as to avoid traffic bottlenecks in a telecommunication network. See e.g. col. 12, line 63 through col. 13, line 24. In Nattkemper, a master switching unit 104a computes the credits awarded to each slave switching unit based on command feedback status cells. Col. 5, lines 24-28. Further, the master switching unit apprises the slave switching units of their computed number of cells for "a given control period." The fairness analysis in the first switching unit 104a is undertaken to compute the credits that each switching unit 104 gets for a given control period." Col. 9, lines 33-36; see also col. 12, lines 65-66 ("The first switching unit 104a operates on a fixed control period....[and] [during this time, the first switching unit 104a computes the credits for each of the other switching units 104a."). When the credits are used up, the slave must waits for "the next control period before launching any more cells." Col. 11, lines 41-43; see also col. 13, lines 19-24 ("Upon receiving the credits,

each slave switching unit 104 starts to launch cells...until its credits are exhausted. The slave switching unit 104 simply remains inactive until the next downstream control cell grants more credits."). At least for this reason, claim 7 and dependent claims 8-13 are allowable.

Method claim 14 has been amended to require, "if the number of empty buffer spaces is larger than a buffer threshold, automatically paying the credit back to the source from which the credit and data were sent." As explained above, the art of record disclose not teach or suggest this combination of limitations. At least for this reason, claim 14 and dependent claims 15-20 are allowable.

Amended claim 21 is directed to a system that that includes a receiver that is adapted to receive memory requests from a plurality of sources. The sources are issued credits issued by the receiver and that receiver "automatically issues a credit to a source without the source having to request a credit." Nattkemper does not disclose automatically issuing credits for providing memory requests as claimed. Shah requires the source to actively request credits. At least for this reason, claim 21 is patentable over the art of record. For at least this same reason, claims 22-24 are allowable as well.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-

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Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,

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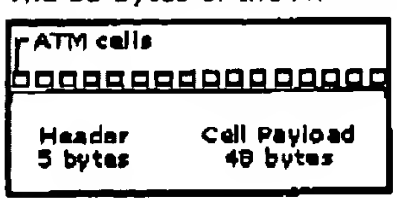
## ATM cells

ATM cells have a fixed length of 53 bytes. Using fixed-length cells, information can be transported in a predictable manner. This predictability accommodates different traffic types (video, voice, data) on the same network.

The 53 bytes of the ATM cell are broken into two principal sections:




Enlarge Figure

- **The header** (5 bytes) is the addressing mechanism, defining how the cell is switched.
- **The payload** (48 bytes), also called the user information field, is the portion that carries the actual information (voice, data, or video).

By using a payload length of 48 bytes for data, ATM offers a compromise between a larger cell size (such as 64 bytes) optimized for data, and a smaller cell size (such as 32 bytes) optimized for voice.